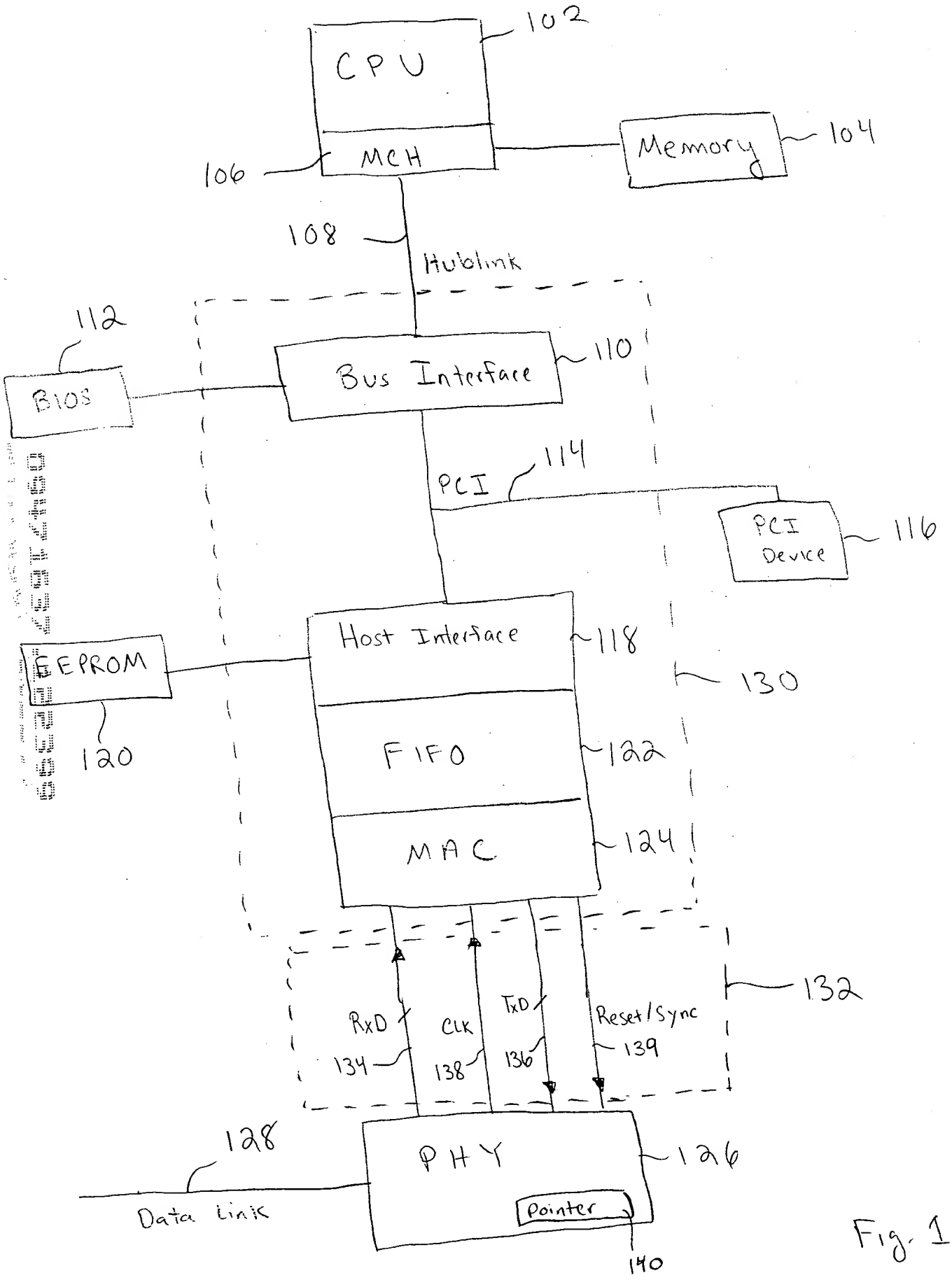
CPU
102
MCH
106
Memory
104
108
Hublink
112
BIOS
Bus Interface
110
PCI
114
PCI Device
116
Host Interface
118
EEPROM
120
130
FIFO
122
MAC
124
132
RxD
134
CLK
138
TxD
136
Reset/Sync
139
128
PHY
126
Data Link
Pointer
140

Fig. 1

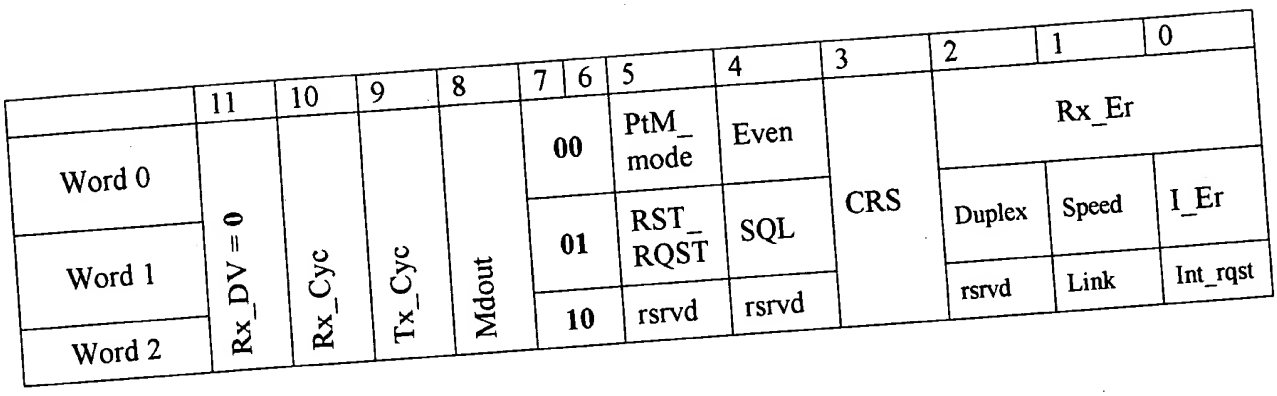
11
10
9
8
7
6
5
4
3
2
1
0
Word 0
Word 1
Word 2
Rx_DV = 0
Rx_Cyc
Tx_Cyc
Mdout
00
01
10
PtM_ mode
RST_ RQST
rsrvd
Even
SQL
rsrvd
CRS
Rx_Er
Duplex
Speed
I_Er
rsrvd
Link
Int_rqst

**Fig. 2**

| 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Rx_Dv = 1 | Rx_Cyc = 1 | Tx_Cyc | Rdata0 | Rdata1 | Rdata2 | Rdata3 | Rdata4 | CRS | Rdata5 | Rdata6 | Rdata7 |

**Fig. 3**

| 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Rx_Dv = 1 | Rx_Cyc = 1 | Mdout | Rdata0 | Rdata1 | Rdata2 | Rdata3 | Rdata4 | CRS | Rdata5 | Rdata6 | Rdata7 |

**Fig. 4**

| 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Rx_Dv = 1 | Rx_Cyc = 0 | Tx_Cyc | Mdout | rsrvd | rsrvd | rsrvd | rsrvd | CRS | rsrvd | rsrvd | rsrvd |

**Fig. 5**

| 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SEL = 0 | Mdstart | Mdin | Tx_EN = 1 | Tdata0 | Tdata1 | Tdata2 | Tdata3 | Tdata4 | Tdata5 | Tdata6 | Tdata7 |
| | | | Tx_EN = 0 | rsrvd | rsrvd | rsrvd | rsrvd | PHY_PD | Lpbk | LED_SEL | Rx_addr_match |
| SEL = 1 | Command_Word | | | | | | | | | | |

**Fig. 6**

| | | | | | |
|---|---|---|---|---|---|
| Mdin | IDLE | ST | OP | Reg Addr (10 bits) | Data (16 bits) |
| | **000...0** | **1** | **01** | | |
| Mdout | IDLE | | | | |

**Fig. 7**

| | | | | | | |
|---|---|---|---|---|---|---|
| Mdin | IDLE | ST | OP | Reg Addr (10 bits) | Wait Time | IDLE |
| | **000...0** | **1** | **10** | | **0001** | **000...0** |
| Mdout | IDLE | | | | **0001** | Data (16 bits) |

**Fig. 8**

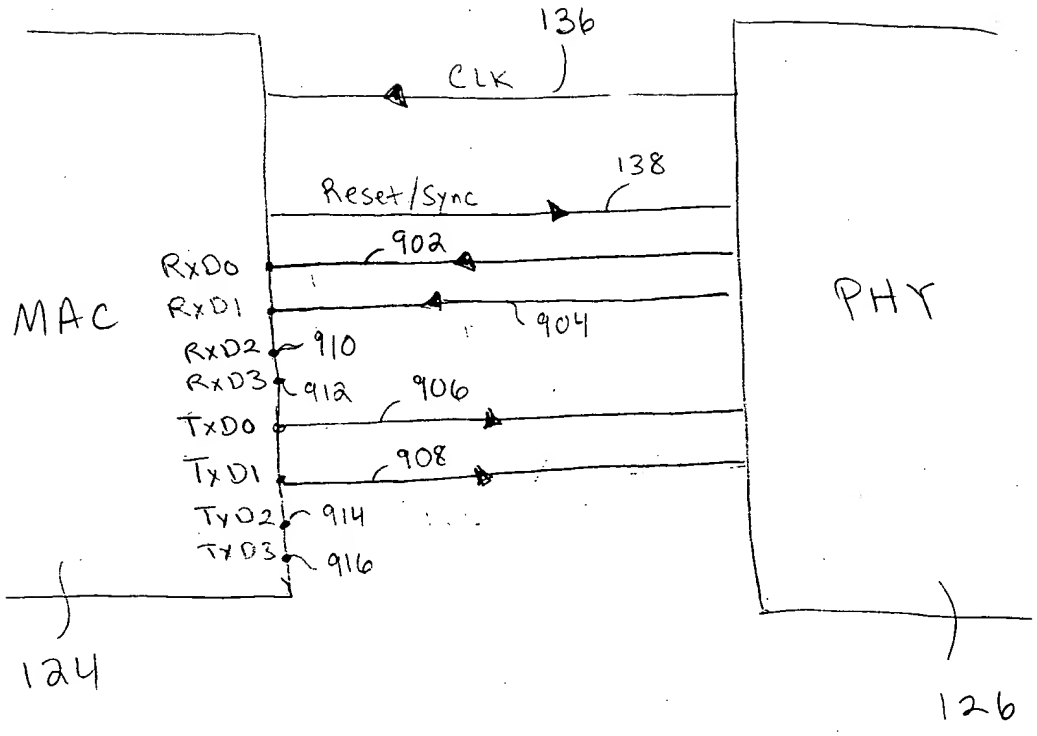
136
CLK
138
Reset/Sync
902
RxD0
RxD1
904
MAC
PHY
RxD2
910
RxD3
912
906
TxD0
908
TxD1
TxD2
914
TxD3
916
124
126

Fig. 9

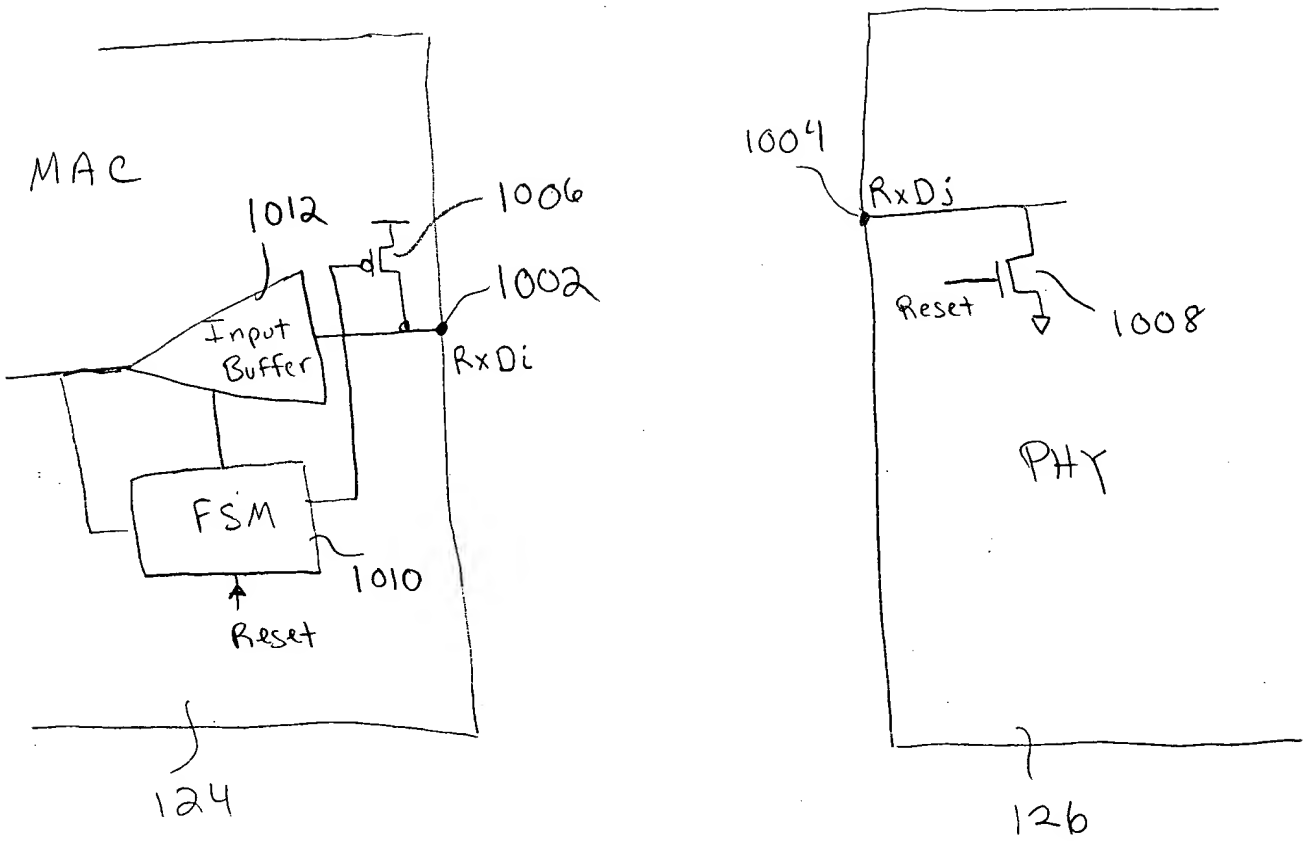
MAC
1012
1006
1002
Input Buffer
RxDi
FSM
1010
Reset
124
1004
RxDj
Reset
1008
PHY
126

Fig. 10

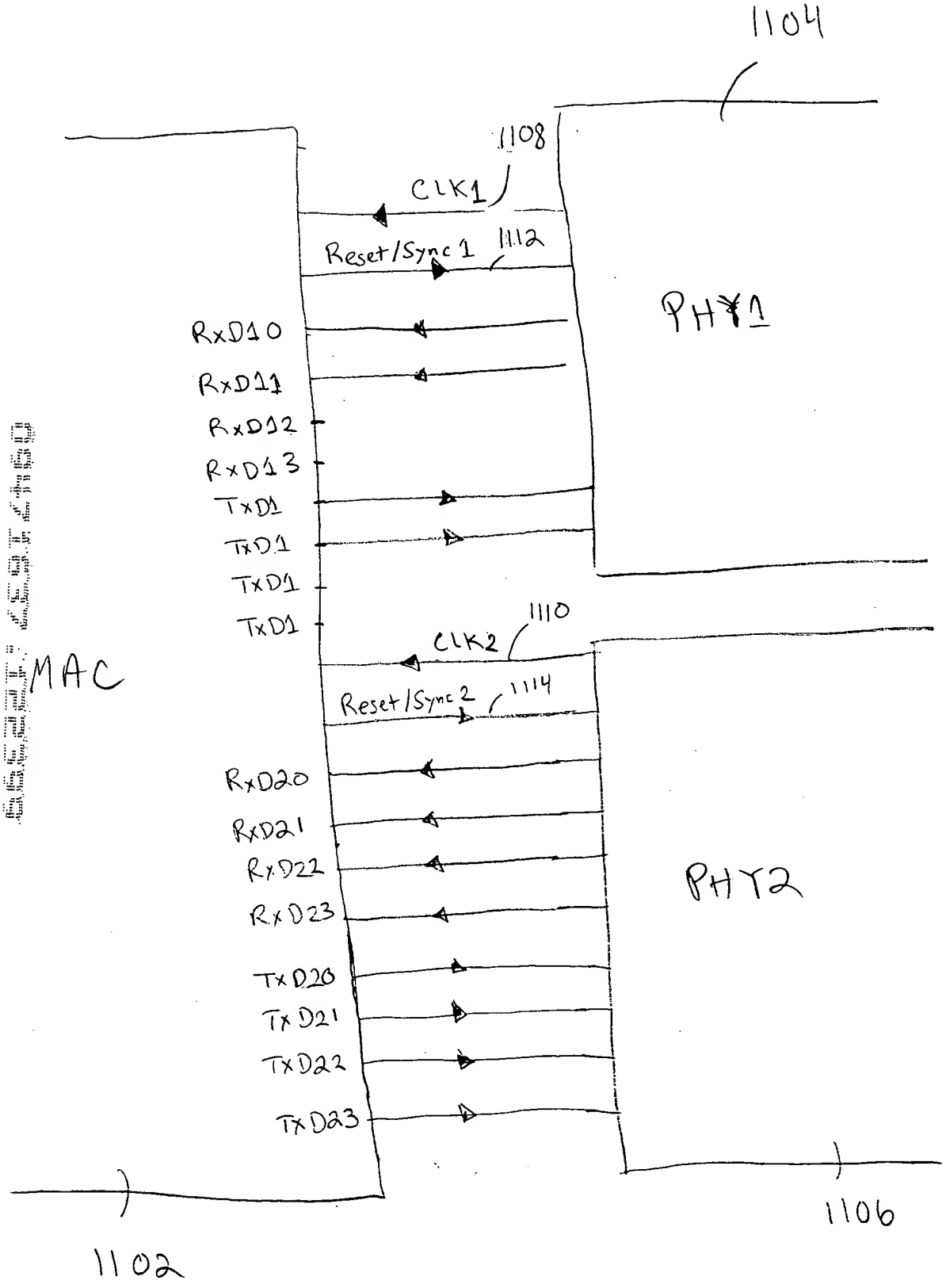
1104
1108
CLK1
Reset/Sync 1
1112
PHY1
RxD10
RxD11
RxD12
RxD13
TxD1
TxD1
TxD1
TxD1
1110
CLK2
Reset/Sync 2
1114
MAC
RxD20
RxD21
RxD22
RxD23
PHY2
TxD20
TxD21
TxD22
TxD23
1106
1102

Fig. 11

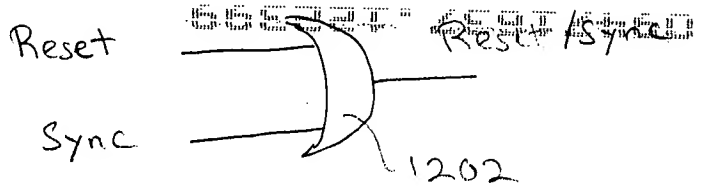


Fig. 12a

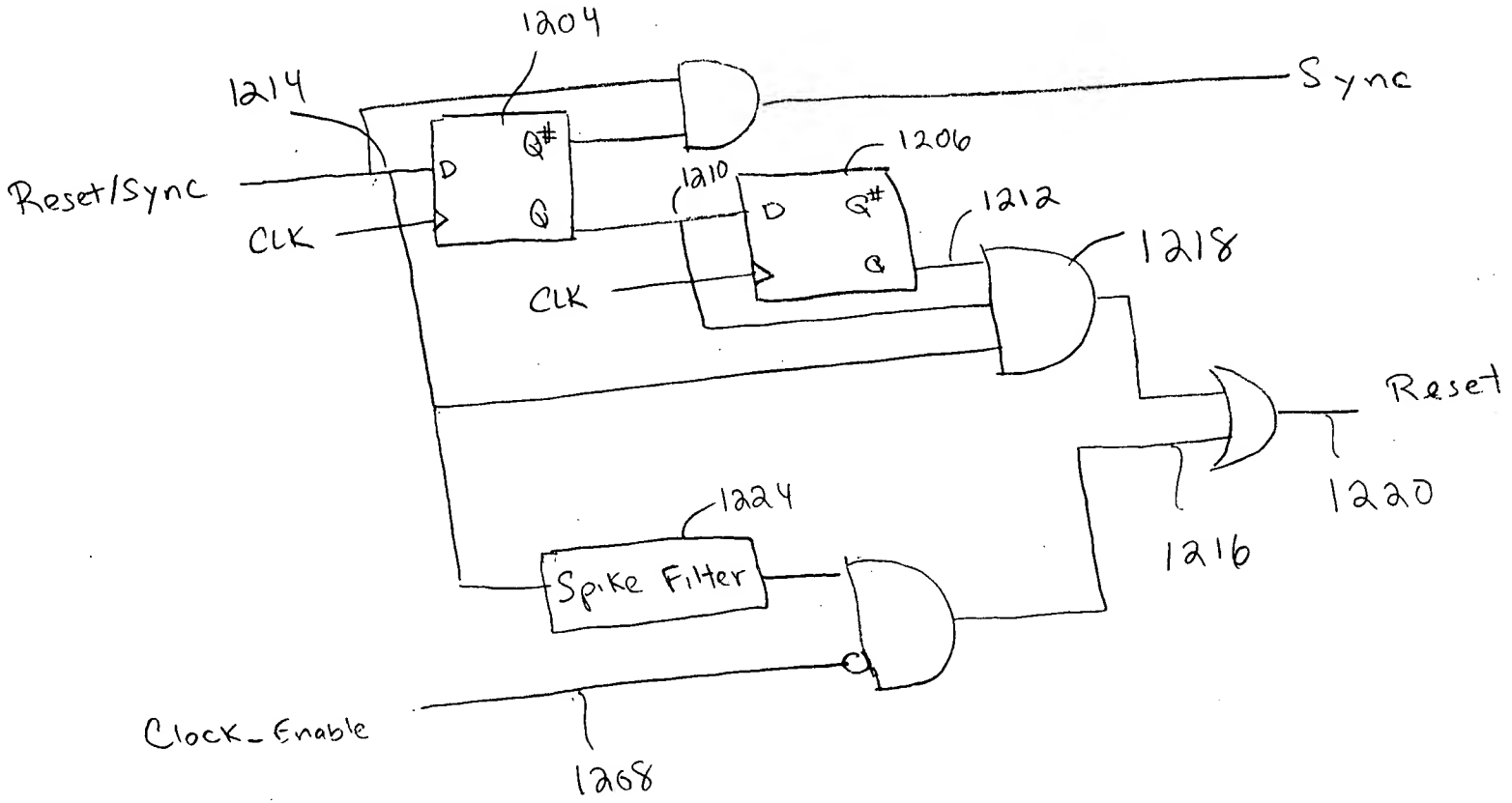


Fig. 12b